Stochastic pulse density modulation for a power LED driver

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Abstract—PWM signals are widely used and easy to implement in a variety of LEDs applications. However, they suffer from significant harmonic generation. As an alternative, SPDM - Stochastic Pulse Density Modulation or SSDM – Stochastic Signal Density Modulation ideas may be considered. The SPDM idea is to spread energy at different frequencies so that it is easier to filter the desired harmonics, because of their lower amplitudes. An example of implementation of SPDM in LED application is presented in the present paper, using a programmable system-on-chip device. Proper operation of the proposed implementation is proved by laboratory results.

Light-emitting diodes (LEDs) are most often controlled by a pulse density modulation signal or in certain cases, direct current. Constant current is particularly needed when all electromagnetic interferences must be eliminated or when stabilizing the LED operating point is of great importance [1÷2]. In the case of digital control, different modulation schemes are utilized to achieve the modulation of LED light intensity. Generally, a desired dimming level is obtained by keeping the proper average duty cycle in a fixed time period. These modulation schemes are part of the main group called pulse density modulation (PDM). The simplest example of the PDM technique is pulse-width modulation (PWM), in which to obtain the desired dimming level, the width of control pulses is modulated.

The simplest analog PWM signal modulator is shown in Fig. 1.

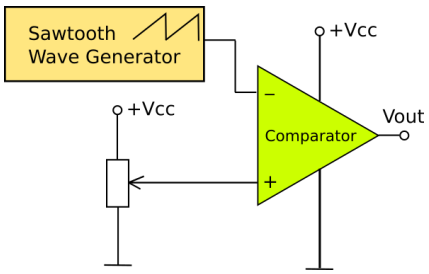

Fig. 1. Block diagram of an analog PWM signal modulator.

The principle of its operation is depicted in Fig 2. The same concept may be utilised in a digital *n*-bit PWM modulator, which is shown in Fig. 3. The modulator consists of a down or up counter and a register which stores the pulse width value.

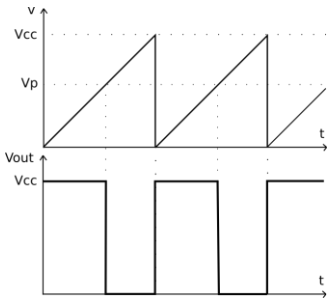

Fig. 2. Principle of operation of the analog PWM modulation.

If a down counter is used, the counter is loaded with the required period, and the pulse width register is loaded with the required dimming value. At each period of the clock signal (which frequency is 2^n times higher than the output PWM frequency), the down counter decrements. In addition, whenever the counter value is less than that of the pulse width register, the comparator output is set to logical "1" level.

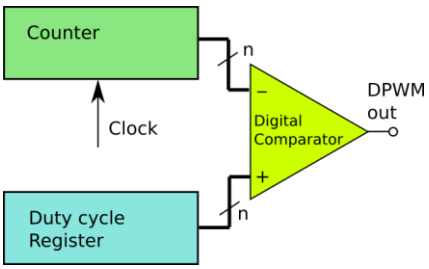

Fig. 3. Block diagram of a digital PWM signal modulator.

For the purpose of controlling LED intensity, the order in which individual pulses occur within a fixed time period is not important. This period, however, must not be longer than about 3 [ms]. It is equivalent of the frequency f_{PWM} = 330 [Hz], which allows to avoid any visible light blinking. What is also important, the total high time or total signal energy in the fixed time frame must be as

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desired. Although PWM is widely used and easy to implement thanks to cheap and easy available microcontrollers, it suffers from significant harmonic generation [3÷5]. What is even worse, the harmonics are generated especially at a relatively low frequency. Because of that, it may require serious filtering, which may be cost and dimension ineffective [6÷8]. As an alternative, the idea of SPDM (Stochastic Pulse Density Modulation or SSDM – Stochastic Signal Density Modulation) may be considered. The idea is to spread energy at different frequencies so that it is easier to filter the desired harmonics because of their lower amplitudes. SPDM uses random (or pseudo random) signal density modulation to generate the average signal density equivalent to the dimming value. Figure 4 shows the basic components of a typical SPDM modulator. For practical utilization of this technique, PSoC (Programmable System-on-Chip) devices seem very attractive.

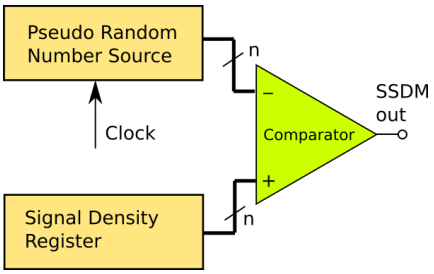

Fig. 4. Block diagram of a digital SSDM / SPDM signal modulator.

PSoC represents an interesting concept in microcontroller architecture. In addition to all the standard elements of typical 8- or 32-bit microcontrollers, the PSoC has digital and analogue freely programmable blocks that allow for the implementation of such peripheral devices, which are only needed in the application. Figure 5 shows the logic diagram of PSoC1 architecture. It contains an M8C PSoC Core, Digital and Analog System, System Resources, Flash and SRAM memories, and an internal 24MHz oscillator. The analogue and digital peripherals can be configured as the designer needs. The stochastic signal density modulation (SSDM) technique is available in PSoC structure as a stand-alone module. Depending on the resolution, it may be composed of one (for 8-bit resolution) to four (for 32-bit resolution) digital blocks. It implements a Stochastic Counter which generates a pseudorandom pack of bits at every tick of the Clock signal, divided by a defined value.

The counter produces randomly ordered codes in the range 1 ... 2^n-1 with a previously declared resolution *n*. This range corresponds to 0 … 100% of the signal density. The resolution setting automatically chooses the correct irreducible polynomial. The Signal Density Register is a *n*-bit register, which after the reset is loaded with a declared signal density value, holds it until a new value is entered. The comparator, over the entire working cycle, compares the current content of the Signal Density Register. If the value of signal density is greater than that of the Stochastic Counter, then the output is in a high logical level. Otherwise, the logical level is low.

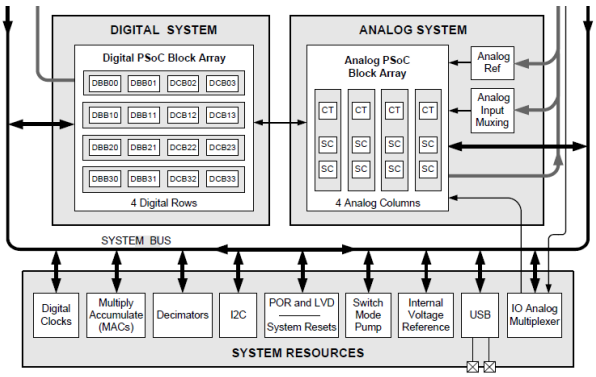

Fig. 5. Simplified structure of PSoC1 [9].

Figure 6 shows an application of 8-bit SSDM in a CY8C27643 microcontroller from the PSoC1 family at the level of project configuration in a dedicated IDE software environment PSoC Designer.

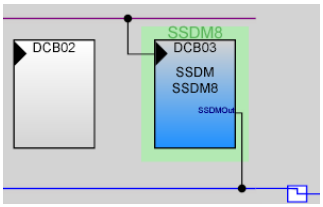

Fig. 6. Design of 8-bit resolution SSDM (one digital block DCBB03).

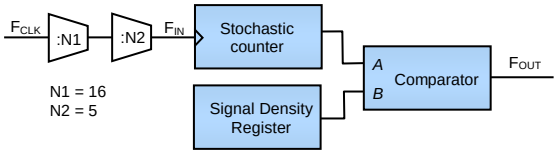

Fig. 7. SSDM illustrative system block diagram.

For the 8-bit resolution, an automatically selected polynomial has the following form: {8,6,5,4} or binary: 1011 1000. Smooth dimming adjustment strongly depends on the minimum and maximum frequencies of the modulation frequency. The first value must be greater than 300Hz, which eliminates the flicker effect, and the second one must be significantly lower than the 2MHz

(operating frequency of the internal controller circuit in the digital configuration).

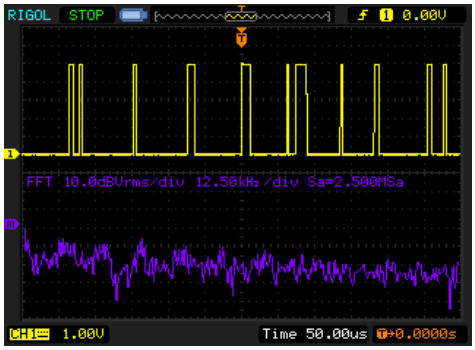

Fig. 8. SSDM signal with density 20%.

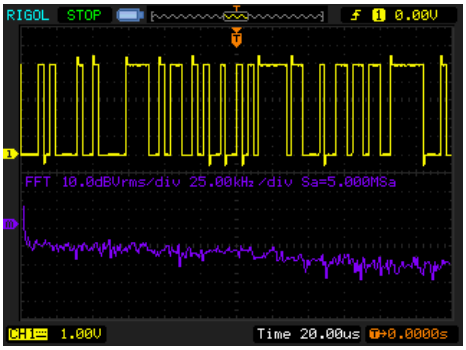

Fig. 9. SSDM signal with density 50%.

The given limit values can be obtained due to an extensive clock signals system. It is assumed that the microcontroller operates at F_{CLK} = 6MHz. This signal is then divided, first by 16 and then by 5 (the largest possible divisor is 16). The input clock signal of the SSDM block is 80kHz. The minimum and maximum frequency value of the output signal can be computed from the following formulas:

$$F_{OUT\ (\min)} = \frac{F_{IN}}{2^n} = 312.5\,Hz\,,\quad F_{OUT\ (\max)} = \frac{F_{IN}}{2} = 40\,kHz \qquad (1)$$

Examples of SSDM waveform and its spectrum plot are shown in Figs. 8÷9. For comparison, the PWM signal and its spectrum is shown in Fig. 10

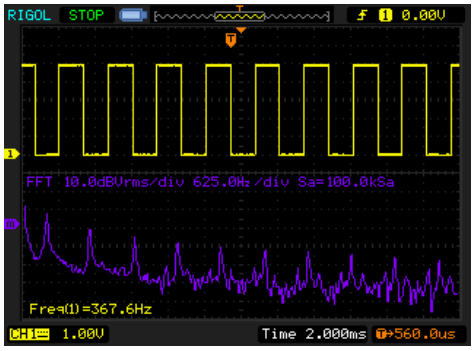

Fig. 10. PWM signal with duty cycle 50%.

Comparing the spectrum shown in Fig. 8÷9 and Fig. 10, it can be concluded that the PWM signal shows the dominant power at the basic frequency and all harmonics except for the DC power. This affects intense striations on these frequencies. The spectrum of an SSDM signal has basically the same power. However, there is no peak value in it. This perfectly illustrates the nature of the SSDM signal spectrum, which should be appreciated when EMI interference is not desired in the target system.

This paper focuses only on demonstrating the ideas and fundamentals of the SSDM method. An insightful and comparative analysis of the described issues, related to the LED control, will be the subject of another publication.

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