Electrical effect of CdSe layer thickness deposited on p- Si wafer

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Abstract—This paper analyzes the current-voltage characteristics of n-CdSe/p-Si heterostructures using experimental data and electrical junction characteristics. To develop n-CdSe/p-Si heterojunctions, a wide band gap semiconducting layer of n-type CdSe thin film has been grown on a p-type Si (100) substrate at 100ºC with different thicknesses using the spray pyrolysis technique. The I-V characteristic of n-CdSe\ p-Si heterostructure has been measured in a room in the dark and under illumination (lamp/160 W). Also, the solar cell IV characteristics and efficiency were measured. The structure's characteristic parameters, such as barrier height, ideality factor, and series resistance, were determined from the current-voltage measurement.

Cadmium selenide (CdSe) is a promising semiconductor material for optoelectronic applications, including thin-film solar cells and light-emitting diodes (LEDs) [1], due to its direct bandgap (1.74 eV) and exciton binding energy (15 meV) at ambient temperature. CdSe is a promising material for optoelectronic applications [2]. There are numerous methods for deposition CdSe thin film, including thermal evaporation [3], chemical vapor deposition (CVD) [4], the sol-gel spin coating process [5], magnetron sputtering [6], chemical bath deposition [7], and spray pyrolysis [8] have been created and employed to fabricate heterojunction structures by growing CdSe thin film on a variety of substrates. The deposition of CdSe film on Si substrate to form a heterojunction is potentially attractive for Photovoltaic (PV) applications [9] because such cells can have an excellent blue light response and be fabricated relatively simply. However, such cells show low energy conversion efficiencies [10–11], and little information is available in the literature. Several models in the literature explained the behavior of the CdSe/Si interface and the characteristics of the current transport across the heterojunction [12–13]. These models include thermionic emission, tunneling (simple and multi-step), space charge region recombination, and minority carrier injection for different fabrication techniques for n-CdSe/p-Si solar cells [14–16].

In this work, the n-CdSe/p-Si heterojunction cell was prepared by spray pyrolysis. We report the n-type behavior of CdSe thin film based on CdSe/p-Si heterojunction solar cells. We describe the electrical properties of CdSe/Si heterojunction solar cells. The present work is likely to be directly comparable and offer a good insight into the behavior of low-cost solar cells.

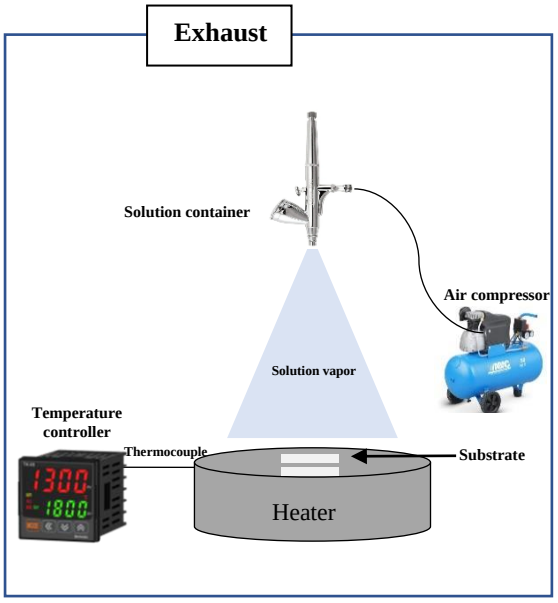

Fig.1. schematic diagram of spray pyrolysis technique.

CdSe/Si heterojunctions were fabricated by using a p-type Silicon wafer with an area 1.0 cm^2 of resistivity 5–10 Ω cm. Silicon wafers ultrasonically were cleaned with Acetone, 2-propanol, and DI water under ultrasonication for 10 minutes each to remove contamination upon the substrate. CdSe film was prepared by using 0.5M of Na_2SO_3 as a Se^+ source and 0.5M of $CdCl_2$ as a Cd^+ source, these two solutions were mixed and freshly sprayed into the Si wafer substrate with 100ºC and symbolled with (js1, js2, js3) respectively depending on the CdSe deposited layers thickness. The film thickness was measured accurately by the gravimetric method. The experimental setup of the chemical spray pyrolysis for the deposition of CdSe thin film is shown in Fig. 1. In each deposition, the nozzle to substrate distance was maintained at 25 cm.

The morphology of thin films of pure CdSe deposited on Si substrate by chemical spray pyrolysis method at 100ºC temperature was examined using a scanning electron microscope (SEM). Figure 2 shows that none of the films are homogeneously distributed or smooth, and the crystallites are between 40–100nm.

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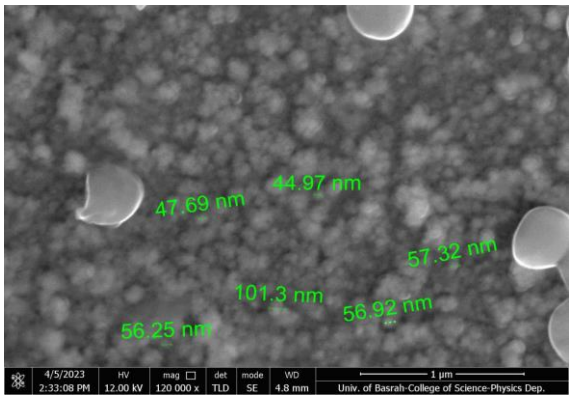

Fig. 2. SEM images of CdSe film deposited on Si wafer.

The schematic structure of the CdSe/p-Si heterojunction is plotted in Fig. 3a. The Au metal contact was deposited on the CdSe layer and the backside of the Si substrate to form electrodes of the p-n diode by the sputtering magnetron method. Current-voltage (I-V) measurements of n-CdSe/p-Si heterojunction diodes were taken at room temperature, in the dark, and under a solar simulator using a Keithley (model 2400) Monochromator /voltage source. The energy band diagram of the structure at equilibrium is shown in Fig. 3b.

The I-V characteristics of the produced samples are described in the literature according to the Thermionic Emission (TE) theory, the forward bias current in non-ideal conditions is expressed as follows:

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right]$$

where I_0 is the reverse-saturation current, q is the electronic charge, V is the voltage value in the forward bias region, n is the ideality factor, k is the Boltzmann constant, and T is the ambient temperature.

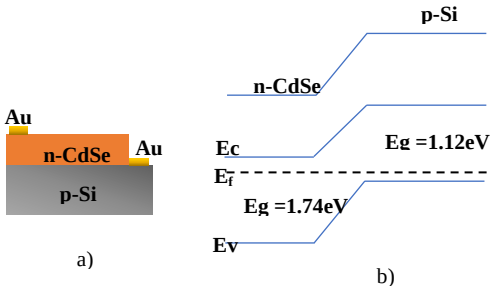

Fig. 3. (a) The schematic structure of the n-CdSe/p-Si heterojunction and (b) the band gap structure of the n-CdSe/p-Si heterojunction.

Figure 4 shows the n-CdSe/p-Si I-V characteristics for the applied bias voltage (forward and reverse) at various CdSe thicknesses. According to this figure's non-linearity of the I-V characteristic curve, thermionic and diffusion mechanisms give rise to the non-ohmic conduction mechanism in nature [17]. The presence of barriers on the device's two sides affords it good rectifying abilities. Based on I-V characteristics, the forward direction features do not significantly differ from those in the reverse direction. This shows that the top and bottom electrodes' (layers') (Si)-(CdSe) interfaces were of a similar type. Following the reduction of interfacial defects and the scattering of carriers at the interface region, as the thickness of CdSe films is increased, the value of the current falls, as shown in Fig. 4 [18]. Additionally, these defects permit the energy levels to reside in the energy gap and function as an active recombination center in the depletion zone, reducing the junction's current flow [19].

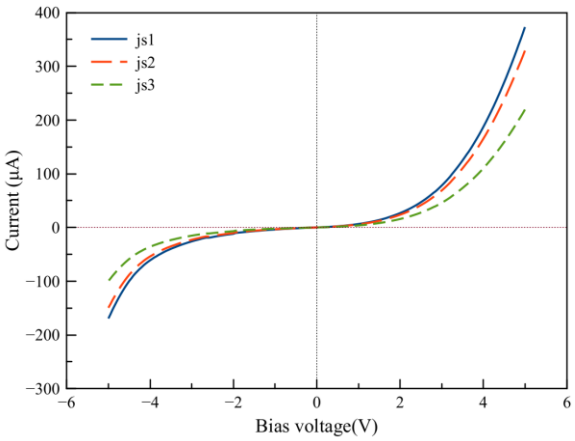

Fig. 4. I-V characteristics in the dark for p-Si/ n-CdSe at different thicknesses of the CdSe layer.

Figure 5 displays the I-V parameters of the cells as determined by illumination measurements at room temperature. It is known that when light is transmitted into an n-CdSe layer, photoelectric effects occur at the p-Si depletion area, particularly close to the heterojunction interface. Band-to-band photoexcitation is not possible in this layer due to the higher bandgap of this layer compared to the Si substrate. A p-Si layer absorbs light, and the produced electrons and holes drift to the positive side of CdSe and the negative side of Si. As a result, photocurrents are obtained. Table 1 illustrates the results of the parameters related to the study, such as I_{sc}, V_{oc}, η of the solar cell, and the thickness of CdSe thin films. It is important to note that the given η value only refers to engineering effectiveness and that neither reflected nor transmitted light was corrected for. However, this efficiency value is comparable to earlier published reports for cells using semiconductor heterojunction devices [20].

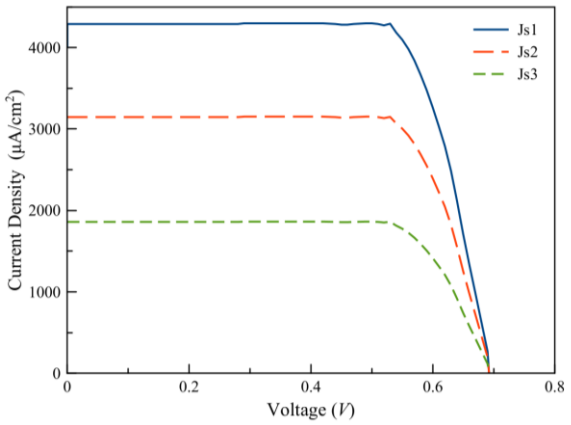

Fig. 5. I-V curve of the p-Si/ n-CdSe heterostructure cell under illumination at different thicknesses of the CdSe layer.

It is evident that the cell's efficiency is low. This may be due to recombining the charges at the depletion zone between the two semiconductors [30]. This might seriously affect the solar cells' ability to operate steadily. The oxidation of the silicon substrate allowed the SiO_2 layer to form due to oxygen passing through the CdSe layer. Therefore, the photocarriers produced in the p-Si depletion zone would have difficulty moving through the n-CdSe layer. As previously noted by Kobayashi et al. [21], this could cause a considerable drop in conversion efficiency. More development of the cells is required to achieve the requirements for actual application.

Table 1-Values of the Short Circuit Current I_{sc}, Open Circuit Voltage V_{oc}, and Efficiency η for the solar cell and solar cell n-CdSe/p-Si

Sample	CdSe Thickness (nm)	I_{sc} (μA)	V_{oc} (volt)	FF	η %
Js1	400	4293	0.53	0.757	4.55
Js2	650	3148	0.54	0.772	3.4
Js3	1037	1860	0.52	0.743	1.93

In conclusion, the n-CdSe/ p-Si cell was prepared by spraying n-CdSe on the p-Si wafer using the chemical spray pyrolysis technique. The current–voltage in the dark and under illumination. The junction exhibits rectifying characteristics with a lower efficiency of about 4.2%. The cell parameters such as open circuit voltage (V_{oc}), short circuit current (I_{sc}), and fill factor (FF) under illumination have also been obtained. The cell exhibited a lower efficiency, which may be due to a recombination of the charges or the structure of the n-CdSe film. However, the aim is the development of low-cost, all-thin-film solar cells where efficiency is also expected to be low.

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