# Reconceiving Impedance Matching and Mismatching to Mitigate Bias-Drift in Insertion Loss of Liquid Crystal Phase Delay Lines

Jinfeng Li,*[1,2,3,4] and Haorong Li[2]

[1]*Advanced Research Institute of Multidisciplinary Science, Beijing Institute of Technology, Beijing, 100081, China,*
[2]*Beijing Key Laboratory of Millimeter Wave and Terahertz, Beijing Institute of Technology, Beijing, 100081, China,*
[3]*Key Laboratory of Short-Range Radio Equipment Testing, Beijing Institute of Technology, Zhuhai, 519088, China,*
[4]*Electrical and Electronic Engineering Department, Imperial College London, London SW7 2AZ, United Kingdom*

Received March 17, 2025; accepted March 26, 2025; published March 31, 2025

**Abstract**—In the microwave (MW), millimeter-wave (mmW), terahertz (THz), and optical beam-steering applications, amplitude imbalance among radiating elements in a phased array antenna feed system can become a point of significance in performance degradation, leading to beam squints, spatial errors, and uneven component lifespans. Higher power consumption in certain elements accelerates material hardening and aging, thereby increasing maintenance costs. This paper proposes a novel, cost-effective hardware approach to mitigate the imbalance of insertion loss in liquid crystal phase delay lines (LC-PDLs). The method compensates for internal losses without relying on feedback loops, thereby eliminating the need for conventional amplifiers or attenuators.

In recent years, there has been a growing market awareness of low-power, continuously tunable beam-steering using liquid crystals (LC) for radiofrequency [1] and photonic [2] applications. This trend has been accelerated by spinouts and startups [3] focusing on LC-based phase-shifting panels for antenna array beam steering. While reducing insertion loss remains a widely studied topic in the research and development of state-of-the-art reconfigurable devices—such as LC-based phase shifters and delay lines [4–5] (as illustrated in Fig. 1)—relatively little attention has been given to amplitude imbalance across different tuning states. In modern beamforming, maintaining amplitude balance between phase-shifting feeds is critical for optimizing both system performance and component longevity in phased array antennas.

Based on the experimentally characterized dielectric response (see Fig. 2) of our iteratively optimized LC-based coplanar waveguide (CPW) phase shifters at 79 GHz under room temperature conditions, the dielectric permittivity (DP) increases from 2.5 to 3.3 as the bias rises from 0 V to 10 V, while the dielectric dissipation factor (DDF) decreases from 0.0123 to 0.0032 over the same voltage range. The phase shifter geometry has been optimized for Merck's GT3-24002 grade of LC, exhibiting a quasi-linear response, thereby mitigating the conventional nonlinearity typically observed in LC-based devices. Regardless of the degree of nonlinearity, the maximum DDF consistently occurs at the lowest DP, corresponding to the lowest bias voltage (0 V), whereas the minimum DDF is observed at the saturated biasing state (e.g., 10 V).

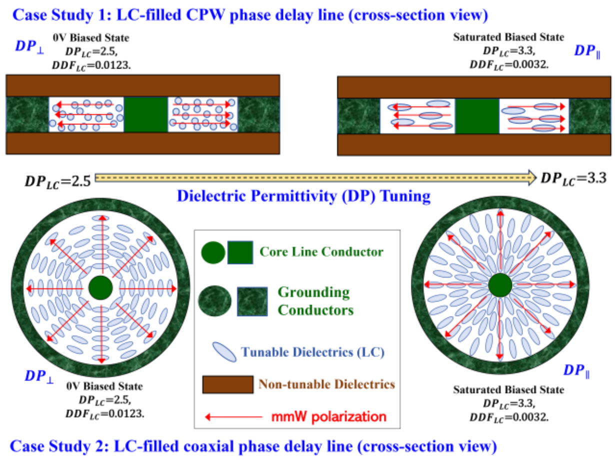


Fig. 1. Cross-sectional illustrations of liquid crystal (LC)-filled coplanar waveguide (CPW) phase delay line (PDL) and coaxial PDL investigated in this study using anisotropic LC (Merck's GT3-24002).

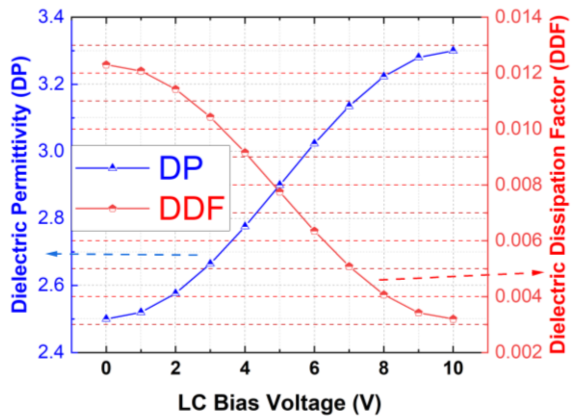


Fig. 2. Characterized dielectric permittivity (DP) and dielectric dissipation factor (DDF) of Merck's GT3-24002 liquid crystal at 79 GHz under room temperature conditions.

* jinfengcambridge@bit.edu.cn

Previous studies and empirical observations [6] indicate that insertion loss is maximized at 0 V bias and decreases significantly as the voltage increases to its saturation level. Consequently, variations in bias voltage led to amplitude imbalances in the transmitted signals across different radiating elements, introducing beam-steering errors and long-term maintenance challenges, as discussed earlier. Fundamentally, the primary contributor to insertion loss is the dielectric loss dissipated within the lossy LC dielectric volume. Since dielectric loss is highly proportional to DDF, which is controlled by the bias voltage, as described by equations derived in [7], bias voltage drift can be considered the dominant factor in amplitude imbalance. Traditional approaches employ feedback loops [8] to regulate the input signal amplitude for self-balancing; however, these additional components introduce increased loss, cost, weight, and system footprint. In contrast, this work utilizes intrinsic passive impedance mismatching as a novel approach to achieve amplitude balancing, eliminating the need for active feedback mechanisms.

This work proposes an elegant approach to eliminate the need for bulky amplifiers or attenuators traditionally used for amplitude compensation. Instead, a combined impedance matching and mismatching strategy is conceptually designed and inherently integrated into the device’s two-dimensional transverse cross-section. By perturbing the matched bias voltage baseline for 50 Ω (see Fig. 3), impedance mismatching is introduced for other bias voltages.

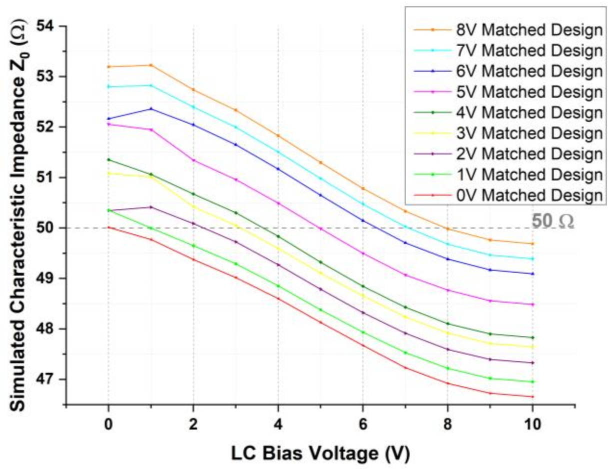


Fig. 3. Principle of proposed insertion loss balancing strategy through perturbation of 50 Ω matching baselines at different bias voltages.

This approach results in a tailored reflection loss profile across different biasing conditions (as illustrated in Figs. 4–6), where reflection loss is intentionally enhanced at the state with the lowest LC DDF and reduced at the state with the highest DDF. Counterintuitively, this mechanism promotes a more balanced insertion loss profile across all biasing states.

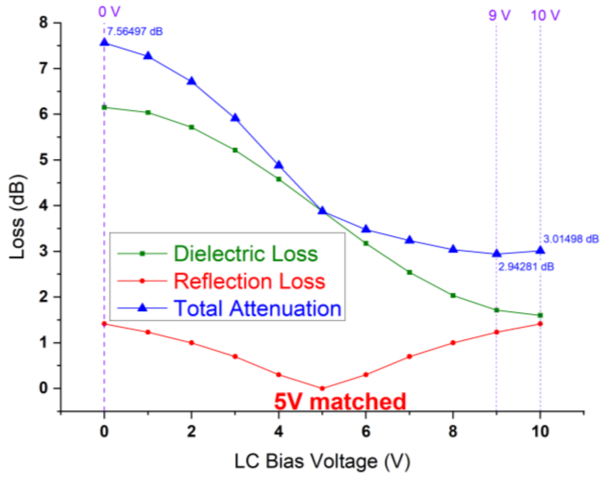


Fig. 4. Numerical loss analysis (79 GHz) for an LC-filled CPW PDL (0–360° differential phase-shifting) design matched at a 5 V bias.

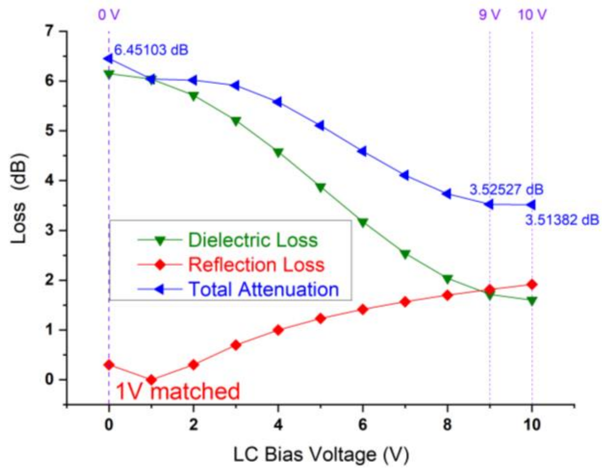


Fig. 5. Numerical loss analysis (79 GHz) for an LC-filled CPW PDL (0–360° differential phase-shifting) design matched at a 1 V bias.

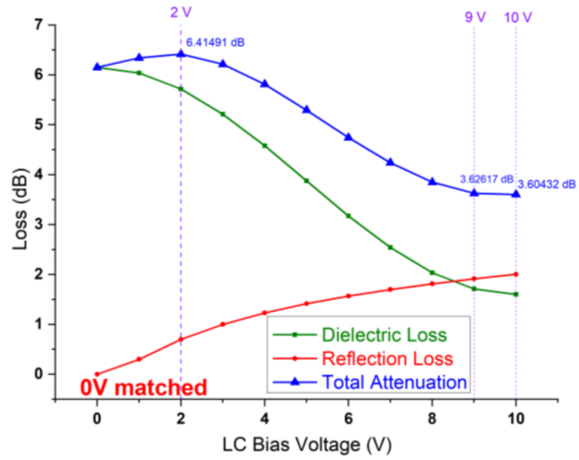


Fig. 6. Numerical loss analysis (79 GHz) for an LC-filled CPW PDL (0–360° differential phase-shifting) design matched at a 0 V bias.

Specifically, designs with impedance-matching baselines perturbed at various bias voltages (ranging from 0 V to 10 V, corresponding to LC permittivity values from 2.5 to 3.3) lead to adaptations in the cross-sectional geometry, including electrode thickness, core line width, and channel width, to achieve 50 Ω impedance. These geometric perturbations, in turn, alter the electric field distribution within the varying dielectric volume and across the modified conductor surfaces, thereby affecting material dissipations such as dielectric loss and metal loss. As demonstrated in the conceptual designs and theoretical analysis presented in Figs. 4–6, the designs matched at 0 V and 1 V exhibit a reduced imbalance (max. ΔIL of 2.81 dB) in the transmitted signal amplitude across the 0 V to 10 V range, whereas the 5 V matched design shows a larger discrepancy (max. ΔIL of 4.62 dB).

Without the need for additional interventions, e.g., amplifiers or attenuators, the proposed simple and cost-effective solution provides high-resolution phase tuning data, while passively bypassing the use of bulky amplitude compensation networks. With this approach in mind, we apply the bias voltage perturbing matching strategy to our recently developed coaxial PDL using the same grade of LC. The key simulated results (see Fig. 7) for the max. insertion loss (max. IL) and the figure-of-merit (FoM), defined as the ratio of the max. differential phase shift to the max. IL, are quantified at 60 GHz using the high-frequency structure simulator (HFSS).

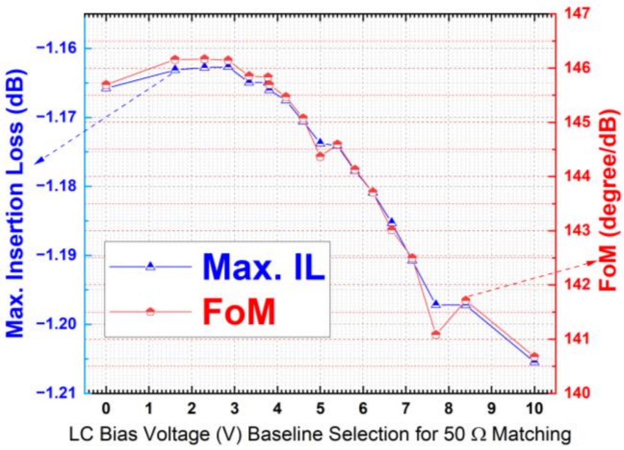


Fig. 7. Maximum insertion loss (IL) and figure-of-merit (FoM) for LC-filled coaxial PDL designs (0–180° differential phase-shifting) with varying bias voltages as 50 Ω matching baselines). Results are numerically re-normalized to 50 Ω to account for reflection loss.

When the baseline is selected at an LC bias voltage of 2.3 V, the figure of merit (FoM) reaches its optimal value of 146.166°/dB, with the max. IL of 1.163 dB at this state. Notably, adjusting the matching baselines within the LC bias voltage range of 0 V to 3 V results in an optimal FoM exceeding 145.693°/dB. However, the FoM decreases when the matching baselines are increased above 4 V, due to a rise in insertion loss. Additionally, low-to-ultra-low variation in insertion loss with tuning voltages is observed. This approach can potentially enable collaborative amplitude-phase modulation at mmW and beyond (e.g., THz), significantly improving the functionality and efficiency of space-time coding metasurfaces.

In summary, the proposed method offers two key benefits: first, it contributes to amplitude balancing, as illustrated in the first case study for the CPW PDL with LC at 79 GHz; second, it mitigates the maximum insertion loss, enhancing the phase shift-to-insertion loss ratio (figure-of-merit), as highlighted in the second case study in Fig. 7 for a coaxial PDL at 60 GHz. This approach reduces the calibration effort, thereby lowering both cost and complexity. The feedback circuit-free solution facilitates large-scale production at a low cost per unit.

While the proposed method shows significant potential for extension to other LC-based tunable delay line topologies and components (e.g., filters, attenuators, resonators, antennas), however, we contend that the impact of the biasing baseline on insertion loss is critically dependent on the wave-occupying-volume-ratio (WoVR) of the tunable dielectrics, which is both geometry- and material-dependent. For coaxial and strip line architectures (with a theoretical WoVR approaching 100% [5,7]), the approach proposed in this work can effectively tip the balance, whereas for structures with relatively lower WoVR, such as the CPW used in the first case study, the perturbed reflection loss may have a less pronounced effect on insertion loss, which is primarily dominated by material absorption. While the proposed method contributes to the direction of insertion loss balancing, achieving a true balance for ultra-precision beam steering targeting a highly performant array gain and interference rejection will require further optimization. Future work will focus on developing a balancing factor to quantify this corrective or regulating effect, tailored to specific transmission line structures at designated frequencies targeting mmW electronics and THz photonics.

This study is supported by the National Natural Science Foundation of China (NSFC Grant 62301043).

## References

[1] J. Li, Crystals **12**, 5 (2022). doi: 10.3390/cryst12050632
[2] U. Chodorow, J. Parka, O. Chojnowska, Phot. Lett. Poland **4**, 3 (2012).
[3] B. Kress, Phot. Lett. Poland **15**, 2 (2023).
[4] J. Li, D. Chu, Crystals **9**, 12 (2019). doi: 10.3390/cryst9120650
[5] J. Li, H. Li, Electronics **13**, 3 (2024). 10.3390/electronics13030626
[6] S. Bulja, D. Syahkal, R. James, S. Day, F. Fernández, IEEE Trans. Microw. Theory Tech. **58**, 12 (2010).
[7] J. Li, H. Li, Crystals **14**, 4 (2024). doi: 10.3390/cryst14040364
[8] D. Brown, *2024 IEEE International Symposium on Phased Array Systems and Technology* (Boston, IEEE 2024). doi: 10.1109/ARRAY58370.2024.10880377